

ABSTRACT OF THE DISCLOSURE

The drain of a power transistor M1 is connected to the non-inverting input terminal of an operational amplifier A and the drain of a transistor M2 is connected to the inverting input terminal of the operational amplifier A to make substantially equal the drain voltages of the power transistor M1 and the transistor M2, of which the gates are connected together and of which the sources are connected together. The drain current of the transistor M2 is outputted via a detection terminal 13 as a current signal proportional to the drain current of the power transistor M1.